University
Digital Logic Module Specification

Course Title: Digital Logic

Credit Hours: 4

Module Leader: Muhammadamin Daneshwar

Module Code: CS207DL

Course Description:
This course provides the student with a foundation in the fundamentals of digital logic design and computer logic circuits. Both combinational and sequential logic circuits are covered in this course. The emphasis is on the use of Boolean algebra and basic logic gates to build cost effective complex logic circuits. Topics include: Number systems, Binary arithmetic, Codes, Logic gates, Boolean algebra and simplifications, Half adders, Full adders, Decoders, Encoders, Multiplexers, Latches, Flip-Flops, Counters, Shift Registers, Memory circuits, and ALU (Arithmetic and Logic Unit).

Course Outline:

1. Introduction to Computer Logic Circuits
2. Number Systems, Binary Arithmetic, and Codes
3. Boolean algebra and Logic Gates
4. The Karnaugh Map and Logic Simplifications
5. Combinational Logic Circuits
a. Half Adders and Full Adders
b. Comparators
c. Encoders and Decoders
d. Code Conversions
e. Multiplexers and De-multiplexers
6. Latches and Flip-Flops
7. Counters
8. Shift Registers
9. Memory Circuits
10. Arithmetic and Logic Unit
11. Hardware Description Language (Verilog)

Learning Objectives:

- ✓ The ability to understand the number system, including binary, octal and hexadecimal numbers, and 2's complement number representation.
- ✓ The ability to understand Boolean algebra and to apply various Boolean theorems to prove Boolean identities and to simplify Boolean functions.
- ✓ The ability to understand the transistor-level structure of TTL and CMOS logic gates and their lectrical and timing characteristics.
- ✓ The ability to construct the K-map from a Boolean expression and to find the minimal SOP/POS forms.

- ✓ The ability to design moderately complex arithmetic and logic circuits including carry lookahead adder, BCD adder, comparator, multiplier, and to evaluate the resulting performance in terms of gate count and propagation delay.
- ✓ The ability to understand the working of MSI devices including decoders, encoders, and multiplexers, and to design various logic circuits using them.
- ✓ The ability to understand the behavior, timing issues, and internal structure of various flip-flops (RS, JK, D and T) and registers.
- ✓ The ability to analyze and design various flip-flop-based state machines (synchronous sequential circuits), including counters.
- ✓ The ability to understand how PLA, ROM, and modern FPGA work and how to use them to design complex logic circuits.
- ✓ The ability to understand the basics of HDL language, to write a HDL program for various logic circuits and to test their functionality and timing.
- ✓ The ability to work in a group. In the lab, students are typically divided into 2-person groups. All lab modules, except the final project, are group efforts graded as a team.
- ✓ The ability to prepare technical documents. There are a number of lab modules in this course. Students are required to submit a comprehensive lab report for each lab module. Lab reports are graded both for technical content and presentation.

Text & References

- ❑ Text Book
- ✓ M. Morris Mano and M. D. Ciletti, Digital Design, 4/e, Pearson Education, 2007.
- ✓ Vahid Frank, Digital Design, Preview Edition, Wiley India Pvt Ltd, 2010
- ❑ **References**
- ✓ R. H. Katz and G. Boriello, Contemporary Logic Design, 2/e,Prentice Hall of India, 2009.
- ✓ A. P. Malvino, D. P. Leach and G.Saha, Digital Principles andApplications, 7/e, McGraw Hill, 2010.
- ✓ S. C. Lee, Digital Circuits and Logic Design, Prentice Hall of India,2006.
- ✓ J. F. Wakerly, Digital Design Principles and Practices, 4/e, PrenticeHall of India, 2000

Marks: The weighting among exams, assignments, and laboratory

- ✓ Final Exam: (20% Practical + 40% Theory)
- ✓ Prefinal: (15% Practical + 25% Theory)
- ✓ 15% Practical includes: in lab activities+reports+ 1 practical exam
- ✓ 25% Theory : Assignment (5%) + 3 Quiz (15%)+ Home work (5%)
- ✓ Note: Students are responsible for adjusting their schedules to take these exams on time. Make-up exams will not be given except in the case of extraordinary circumstances (such as death of a family member or significant traffic accident) proven with formal documents or other issue singed by Head of Computer Department.

Authored by

Muhammadamin Daneshwar, 21/09/2014

Validated and Verified by